SCAS162B - JUNE 1990 - REVISED NOVEMBER 1996

- Members of the Texas Instruments Widebus™ Family
- Inputs Are TTL-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC[™] (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Packages Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Packages Using 25-mil Center-to-Center Pin Spacings

description

The 'ACT16863 are 18-bit noninverting transceivers designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

The 'ACT16863 can be used as two 9-bit transceivers or one 18-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the output-enable (OEAB or OEBA) inputs.

54ACT16863 . . . WD PACKAGE 74ACT16863 . . . DL PACKAGE (TOP VIEW)

		U		1
1OEAB	1		56	1 <mark>OEBA</mark>
1B1	2		55] 1A1
1B2	3		54] 1A2
GND [4		53	GND
1B3 🛚	5		52] 1A3
1B4 [6		51] 1A4
v _{cc} [7		50] v _{cc}
1B5 [8		49] 1A5
1B6 [9		48] 1A6
1B7 [10		47] 1A7
GND [11		46	GND
1B8 [12		45] 1A8
1B9 [13		44] 1A9
GND [14		43	GND
GND [15		42	GND
2B1	16		41] 2A1
2B2	17		40] 2A2
GND [18		39	GND
2B3	19		38] 2A3
2B4	20		37] 2A4
2B5 [21		36] 2A5
v _{cc} [22		35] v _{cc}
2B6 [23		34] 2A6
2B7	24		33] 2A7
GND [25		32	GND
2B8	26		31] 2A8
2B9	27		30	2 <u>A9</u>
2OEAB	28		29	2 <mark>OEBA</mark>

The 74ACT16863 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16863 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT16863 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE (each 9-bit section)

INP	UTS	
OEAB	OEBA	OPERATION
Н	L	B data to A bus
L	Н	A data to B bus
Н	Н	Isolation



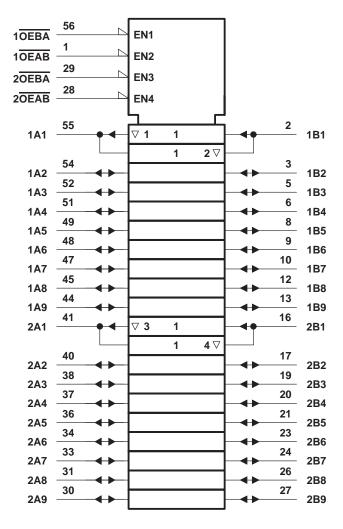
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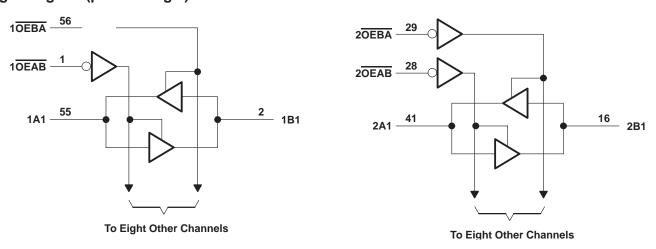
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logic symbol†



 $[\]dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC}	0.5 V to 7 V
Input voltage range, V _I (see Note 1)—C	$0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Output voltage range, V _O (see Note 1)C	$0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }$ ($V_{ C }$ or $V_{ C }$ $V_{ C }$	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V _{CC} or GND	±450 mA
Maximum package power dissipation at $T_A = 55^{\circ}C$ (in still air) (see Note 2): DL package	1.4 W
Storage temperature range, T _{stq}	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 2)

		54	ACT1686	33	74	ACT1686	33	UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
VIH	High-level input voltage	2		7	2			V
V _{IL}	Low-level input voltage		Š	0.8			0.8	V
٧ _I	Input voltage	0	2	VCC	0		VCC	V
Vo	Output voltage	0	7	VCC	0		VCC	V
IOH	High-level output current		2	-24			-24	mA
lOL	Low-level output current	20	5	24			24	mA
Δt/Δν	Input transition rise or fall rate	0		10	0		10	ns/V
TA	Operating free-air temperature	-55		125	-40		85	°C

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

54ACT16863, 74ACT16863 18-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DA	RAMETER	TEST CONDITIONS	\	T,	<u> </u> = 25°C	;	54ACT	16863	74ACT	16863	UNIT	
PA	RAWEIER	TEST CONDITIONS	Vсс	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNII	
		Jan - 50 uA	4.5 V	4.4			4.4		4.4			
		IOH = -50 μA	5.5 V	5.4			5.4		5.4			
V/0		10.1 - 24 mA	4.5 V	3.94			3.7		3.8		V	
VOH		I _{OH} = −24 mA	5.5 V	4.94			4.7		4.8		V	
		I _{OH} = -50 mA [†]	5.5 V				3.85					
		I _{OH} = -75 mA [†]	5.5 V						3.85			
I _{OL} = 50 μA		4.5 V			0.1		0.1		0.1			
		ΙΟΣ = 30 μΑ	5.5 V			0.1		0.1		0.1	٧	
V/01		lo 24 mA	4.5 V			0.36	4	0.5		0.44		
VOL		I _{OL} = 24 mA	5.5 V			0.36	(0)	0.5		0.44		
		I _{OL} = 50 mA [†]	5.5 V				$g_{Q_{\zeta}}$	1.65				
		$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V				A.		1.65			
Ц	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μΑ	
loz‡	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±10		±5	μΑ	
ICC	•	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		160		80	μΑ	
ΔlCC§	One input at 3.4 V, Other inputs at V _{CC} or GND		5.5 V			0.9		1		1	mA	
Ci	Control inputs	V _I = V _{CC} or GND	5 V		4.5						pF	
C _{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		17						pF	

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	ROM TO		T _A = 25°C			16863	74ACT	UNIT		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	ONIT	
t _{PLH}	A or B	B or A	4.1	7	9.9	4.1	12.1	4.1	11.1	nc	
^t PHL	AUIB	BUIA	3.1	6.4	10.6	3.1	12.5	3.1	11.8	ns	
^t PZH		A or B	3	5.9	9.6	3	11.5	3	10.6	20	
^t PZL	OEBA or OEAB	AUID	3.9	7.4	12.3	3.9	14.7	3.9	13.6	ns	
^t PHZ	OF DA OF A D	A or B	5.7	8.2	10.6	5.7	12.3	5.7	11.6		
t _{PLZ}	OEBA or OEAB	AUB	5.4	7.7	10	5.4	11.6	5.4	11	ns	

operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

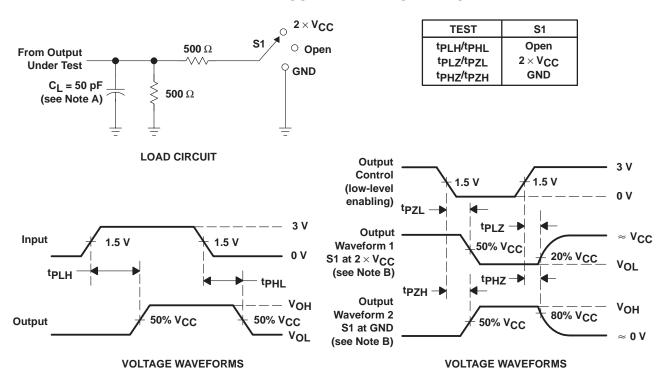
	PARAMETER	TEST CO	TYP	UNIT		
C _{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50 \text{ pF},$	f = 1 MHz	62	pF



[‡] For I/O ports, the parameter IOZ includes the input leakage current.

[§] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f = 3$ ns. $t_f = 3$ ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ACT16863DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT16863DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT16863DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74ACT16863DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





Α	0	Dimension designed to accommodate the component width
В	0	Dimension designed to accommodate the component length
		Dimension designed to accommodate the component thickness
٧	٧	Overall width of the carrier tape
ГР	1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ACT16863DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74ACT16863DLR	SSOP	DL	56	1000	346.0	346.0	49.0

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